Development of a FPGA based PCI-express to optical link interface card, KINPEX

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A new PCI-express (PCIe) to optical link interface card, KINPEX, has been designed and produced to replace a current PCIe card, PEXOR[1]. It provides high speed data transfer from front-end cards to standard personal computers (PC) to support experiments with high data rates at FAIR. Both cards are equipped with a high performance FPGA to control the whole system, a four-lane PCIe bus and four small form-factor pluggable (SFP) transceivers. For the KINPEX card, we have adapted Kintex-7 FPGA from Xilinx corp. for price-performance reason, while SCM40 FPGA from Lattice Semiconductor corp. was chosen for the PEXOR card at 2008. Detailed hardware specification is available from the reference [2].

Figure 1: KINPEX, a PCIe to optical link interface card.

The new FPGA firmware to operate the KINPEX card has been developed. It supports data exchange with a PC via PCIe bus, which is realized with the serial interconnect building block of the FPGA configured by an intellectual property (IP) core from the manufacturer. It is configured with a per lane data rate of 2.5 GT/s to be compatible with PEXOR. The IP core supports the physical, data link, and transaction layers of PCIe protocol and gives an example to process transaction layer packets (TLPs). The example was modified to perform 32-bit memory read/write access to control registers and four 256 KByte dual-port memories (DPMs) prepared for storage of data from SFPs. For the maximum data throughput, the DMA engine developed for PEXOR is utilized for KINPEX [1]. It provides maximum payload size of 128 bytes and performs two modes of data transfer. One transfer mode waits arrival of complete data to the DPMs from SFPs, before it sends data to the PC from each DPM in sequence. The other transfer mode is able to activate only one of the four SFPs, however it performs DMA data transfer via a FIFO memory as soon as stored data reaches payload size of 128 bytes.

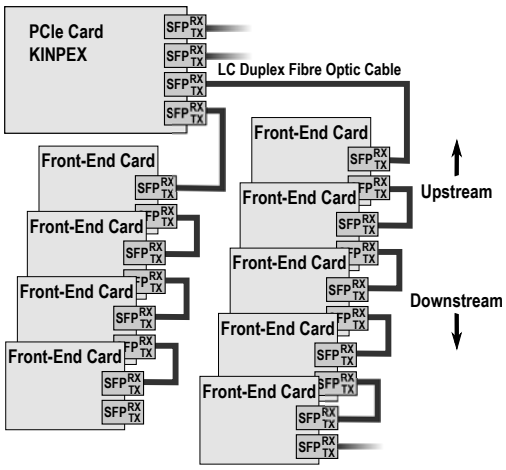

Figure 2: Connection of the PCIe card and the front-end cards.

The firmware supports communication with front-end cards via SFPs with GOSIP (gigabit optical serial interface protocol)[3]. It is a master and slave protocol with two modes of data transfer, address and block mode, and the main feature is that one SFP port of master is capable to control multiple slaves equipped with 2 SFPs. The front-end cards (slaves) can be chained in a way that one SFP of the front-end card upstream can be connected with the other SFP of the one downstream as shown in figure 2. Payload of data is kept as 1.6Gbps per SFP as PEXOR is.

The standard data acquisition (DAQ) system at GSI, Multi-Branch System (MBS) [4], has been upgraded to support the KINPEX cards and the system with the KINPEX card is working stable with expected performance.

References

[1] J. Hoffmann *et al.* GSI Scientific Report 2008, p275

[2] `https://www.gsi.de/fileadmin/EE/Module/Dokumente/kinpex1_pcb15.pdf`

[3] S. Minami *et al.* IEEE Trans. Nucl. Sci., vol. 58, no. 4, pp. 1816-1819, Aug. 2011

[4] H.G. Essel and N. Kurz, IEEE Trans. Nucl. Sci., vol. 47, no. 2, pp. 337-339, Apr. 2000

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